IN THE SPECIFICATION

Please insert the following replacement paragraph starting at Page 9, line 9 of the specification:

Referring initially to Fig. 2, the main unit interface 10a is illustrated. The joint electrical interface between the main unit 10 and the option pack 12 is illustrated as block 50. The joint electrical interface 50 refers to the coupled state of the main unit connector 36 and the option pack connector 38. The address signals 52, the data signals 54, and control signals, such as memory or I/O control signals 56 and PCMCIA control signals 58 from the processor 60, may be electrically coupled through the interface 50 through isolation buffers 62. The main unit 10 also includes system memory 63 for stroing applications, associated drivers and data. The isolation buffers 62 may be bi-directional for bi-directional signals, or unidirectional for unidirectional signals. The logic flow of the isolation buffers 62 may be controlled by a Programmable Logic Device (PLD) 64. The main unit interface 10a may also comprise a micro-controller 66 configured to receive serial data on a Universal Asynchronous Receive and Transmit (UART) data bus 68. The main interface unit 10a may also be configured to transmit data on a Serial Peripheral Interface (SPI) data bus 70 to provide initial handshaking between the main unit 10 and the option pack 12. The low-level handshaking associated with the micro-controller 66 facilitates the exchange of identification data between the main unit 10 and the option pack 12. The SPI bus 70 also provides serial access for battery monitoring and charge control on the option pack 12. The option pack interface 12a may comprise an SPI EEPROM which provides for identification of the option pack 12 and the features it offers, as discusses with reference to Fig. 3.